AF/2813/8

Appeal Brief OKOW 5/6/03

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Docket No. AF01120 **PATENT**

In re Appellants:

Halliyal, et al.

Serial No: 10/023,548 Art Unit: 2813

Filed: December 17, 2001 Examiner: Erik J. Kielin

For: INTEGRATED ONO PROCESSING FOR SEMICONDUCTOR DEVICES USING IN-SITU STEAM GENERATION (ISSG) PROCESS

APPEAL BRIEF

Commissioner of Patents
Washington, DC 20231

Dear Sir:

This Appeal Brief is submitted, in triplicate, in the above-identified application in response to the final Office Action mailed December 19, 2002. Appellants' Notice of Appeal was received in the Office on April 09, 2003, with a one-month extension of time for responding to the final Office Action. Accordingly, Appellants' Appeal Brief is timely filed, with no extension of time.

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Dear Sir:

This Appeal Brief is submitted, in triplicate, in the above-identified application in response to the Office Action mailed December 19, 2002, in furtherance of the Notice of Appeal which was received in the Office on April 09, 2003.

I. REAL PARTY IN INTEREST

The real parties in interest in this appeal are (1) Advanced Micro Devices, Inc., One AMD Place, Sunnyvale, California 94088; and (2) Fujitsu Limited, 1-1 Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa-ken, Japan.

II. RELATED APPEALS AND INTERFERENCES

Appellants are aware of no related appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-21 are presently pending in the Application. Claims 2-4, 14-16 and 18-21 were withdrawn from consideration on the basis of an election of species requirement imposed by the Examiner. (Claim 17 should have been included in this group, but was erroneously made dependent on claim 12 instead of claim 14. Claim 17 was amended to correct this error, and was thereafter included with the claims dependent on claim 14.) However, in the final Office Action, the Examiner, with no explanation or reason, asserted that "newly submitted claims 14-21 [are] directed to an invention that is independent or distinct from the invention originally claimed". The Examiner also asserted, with no explanation or reason, that claim 1 is no longer generic to claims 14-21. Appellants have requested all of the withdrawn claims be reinstated, since claim 1 is in fact generic and, as Appellants show herein, claim 1 is allowable. The bases for Appellants' position with respect to the generic nature and allowability of claim 1 are set forth hereinbelow. Claims 1 and 5-13 stand finally rejected, and claims 2-4 and 14-21 stand withdrawn, for which Appellants bring the present appeal to the Board. The Appendix contains a copy of all of claims 1-21, all of which are considered by Appellants to be involved in this appeal.

IV. STATUS OF AMENDMENT

An amendment under 37 C.F.R. 1.116(a) was filed in this application, and the Examiner issued an Advisory Action. Thus, at the present time, there is no amendment pending. A second amendment 37 C.F.R. 1.116(a) is filed together with this Appeal Brief, to correct a typographical error in claim 18. This amendment does not substantively change the scope of claim 18. The amended form of claim 18 is set forth in the Appendix.

V. SUMMARY OF INVENTION

Appellants' invention, in one embodiment, relates to a process for fabricating a semiconductor device including an oxide-nitride-oxide (ONO) structure, including forming the ONO structure by providing a semiconductor substrate which has a silicon surface,

forming a first oxide layer on the silicon surface, depositing a silicon nitride layer on the first oxide layer, and forming a top oxide layer on the nitride layer, thereby forming an ONO structure. P. 3, l. 27 to p. 4, l. 2. Both the first oxide layer and the top oxide layer are formed by in-situ steam generation (ISSG) oxidation of the layer on which the respective oxide is being formed. P. 11, ll. 1-4, and p. 12, ll. 21-23. Thus, a first ISSG oxidation is applied to the silicon surface of the semiconductor substrate to form the first oxide, and a second ISSG oxidation is applied to the surface of the silicon nitride layer to form the top oxide layer. *Id.* In one embodiment, the semiconductor device is specified to be a two-bit EEPROM device, and the first oxide layer is referred to as a tunnel oxide layer. P. 4, ll. 3-9. In another embodiment, the semiconductor device is specified to be a floating gate FLASH structure, and the first oxide is referred to as a bottom oxide. P. 4, ll. 10-17. As noted on page 4, lines 18-30, the present invention, by use of an ISSG oxidation of a silicon nitride layer formed in-situ, an ONO layer may be fabricated without creation of interface states coming from contamination which could provide charge leakage paths within the ONO structure. This same benefit accrues to the first oxide layer formed on the silicon surface of the semiconductor substrate. The present invention provides advantages such as (1) formation of a cleaner interface between the oxide layers formed and the underlying layer, including less carbon; (2) use of ISSG oxidation, which is faster than other oxidations, thus requiring a lower thermal budget; and (3) formation of a sharper nitride/top oxide interface, resulting in fewer interface states that could provide charge leakage paths within the ONO structure. *Id.*

VI. ISSUES ON APPEAL

The claims on appeal stand rejected under 35 U.S.C. §§ 103(a). The issues in this appeal are as follows.

A. THE UNOBVIOUSNESS OF CLAIMS 1 AND 5-13 OVER OKUYAMA ET AL, U.S. PATENT NO. 4,918,503, IN VIEW OF VAN ZANT, MICROCHIP FABRICATION, pp. 172-173, 179-182 AND 480-487.

B. THE GENERIC NATURE OF CLAIM 1 REQUIRES THAT CLAIMS 2-4 AND 14-21 BE INCLUDED IN THE EXAMINED CLAIMS, UPON A FINDING THAT CLAIM 1 WOULD NOT HAVE BEEN OBVIOUS OVER THE ASSERTED PRIOR ART IN (A).

C. THE UNOBVIOUSNESS OF CLAIMS 2-4 AND 14-21 OVER OKUYAMA ET AL, U.S. PATENT NO. 4,918,503, IN VIEW OF VAN ZANT, MICROCHIP FABRICATION, pp. 172-173, 179-182 AND 480-487.

D. THE EXAMINER APPLIED AN IMPROPER STANDARD OF, AND FAILED TO PROPERLY STATE A CASE OF OBVIOUSNESS.

VII. GROUPING OF CLAIMS

Appellants' claims can be grouped into three groups, claim 1 and the claims dependent thereon, claim 14 and the claims dependent thereon, and claim 18 and the claims dependent thereon. Thus, claims 1-13 stand or fall together, claims 14-17 stand or fall together, and claims 18-21 stand or fall together. Since claim 1 is generic to claims 14 and 18, if claim 1 is found to be allowable, the remaining claims should be allowable as well.

VIII. ARGUMENT

A. CLAIMS 1 AND 5-13 ARE UNOBVIOUS AND PATENTABLE OVER OKUYAMA ET AL, U.S. PATENT NO. 4,918,503, IN VIEW OF VAN ZANT, MICROCHIP FABRICATION, pp. 172-173, 179-182 AND 480-487.

Claims 1 and 5-13 stand rejected under 103(a) as obvious over US 4,918,503, Okuyama et al., in view of Van Zant, Microchip Fabrication. The Examiner asserted that Okuyama et al. discloses a process such as that claimed, but admitted that Okuyama et al. fails to indicate the method by which steam oxidation is performed. The Examiner cited Van Zant for the substitution of ISSG oxidation for the steam oxidation of Okuyama et al. Appellants respectfully traverse the rejection over these references on the following grounds.

In summary, Appellants respectfully submit the Examiner failed to state a legally correct *prima facie* case of obviousness. The cited references fail to disclose all the limitations of Appellants' claims, and fail to provide any legally cognizable suggestion or motivation for making the modifications which would be necessary to reach Appellants' claimed invention. The Examiner's attempts to show all of the limitations and the asserted motivation are legally incorrect and without proper evidentiary basis.

The Examiner failed to identify at least two specifically recited limitations of Appellants' claimed invention in the prior art. The first missing limitation relates to formation of the first oxide layer. Appellants' claims specify that the first oxide layer is formed on the silicon surface of a semiconductor substrate; i.e, the first oxide is formed on the substrate. Okuyama et al. does not disclose formation of an oxide layer on the substrate. Instead, Okuyama et al. discloses formation of two intermediate layers on the substrate, and thereafter formation of an oxide layer over the second intermediate layers. To wit, at col. 4, lines 28-41, Okuyama et al. discloses that a P+-type layer 46 and an N+-type layer 45 are formed on the substrate 11, and that the first oxide layer 14 is formed not by steam oxidation of the substrate, but "through a heat treatment of 900°C under dry oxygen atmosphere, the first silicon oxide film 14 is formed." Thus, the first oxide layer 14 is not formed on the substrate 11 as claimed in Appellants' claims, but rather it is formed on an N+-type layer 45 which is on a P+-type layer 46, which in turn is on the substrate 11.

These layers are shown in detail in Figs. 2A, 2B and 2C of Okuyama et al., which in each case include the layers 45 and 46 separating the oxide layer 14 from the substrate 11. For the convenience of the Board, Figs. 2A, 2B and 2C are reproduced above and below. It is quite clear from Fig. 2A of Okuyama et al. that the oxide layer 14 is separated from the substrate 11 by not just one, but two layers, N+-type layer 45 and P+-type layer 46. Thus, the first oxide layer formed by Okuyama et al. is not formed on the silicon surface of the semiconductor substrate, as claimed by Appellants' claim 1.

Like Fig. 2A, Figs. 2B and 2C clearly show the same two layers, N+-type layer 45 and P+-type layer 46, between the oxide layer 14 and the silicon surface of the semiconductor substrate 11. Figs. 2B and 2C are plan views of two embodiments of

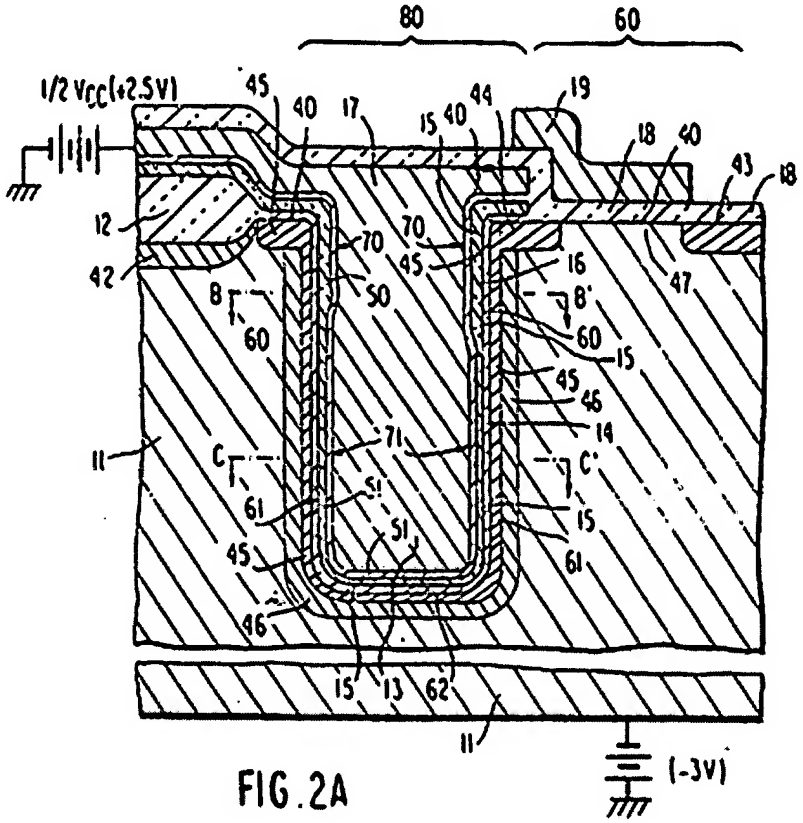


FIG. 2A

Okuyama et al. specifically referred to by the Examiner. The Examiner correctly noted that the layers 14, 15 and 16 constitute oxide, nitride, oxide layers, respectively. However, the Examiner failed to show that the first oxide deposited, layer 14, is deposited on the silicon surface of the substrate 11. In fact, as clearly shown in both Figs. 2B and 2C, the layer 14 is deposited on layer 45, which is in turn formed on layer 46, and only layer 46 is formed on the substrate 11. Figs. 2B and 2C clearly show that the oxide of Okuyama et al. is not formed on the surface of the substrate 11. Okuyama et al. specifically describe forming the two layers, N+-type layer 45 and P+-type layer 46, as separate steps, prior to forming the oxide layer. Thus, Okuyama et al. discloses a structure formed by a process quite distinct form the presently disclosed and claimed process.

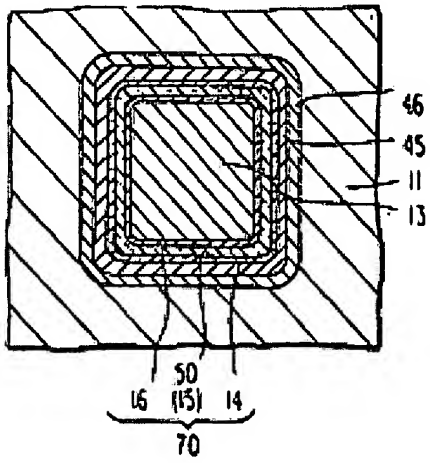
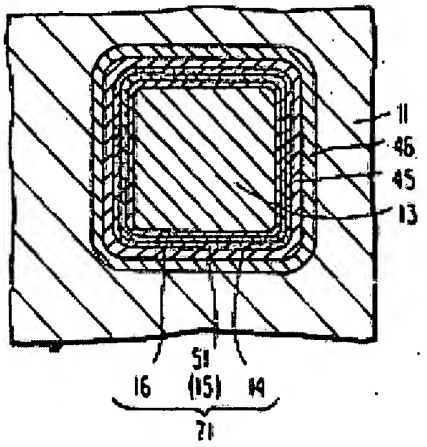


FIG.2B

FIG.2C



While the Examiner might argue that the P+-type layer 46 constitutes "a silicon surface", such a silicon surface is not a surface of the substrate 11, it is a surface of a layer, P+-type layer 46, which has been formed on the surface of the N+-type layer 45, which in turn has been formed on the surface of the substrate 11. It is factually incorrect to state that the oxide layer 14 is formed on the substrate 11. Thus, even a broad reading of Appellants' claims does not reach the structure disclosed by Okuyama et al. Okuyama et al. simply does not disclose an oxide layer formed as claimed. For this reason, Okuyama et al., even with the disclosure of Van Zant, could not have rendered obvious Appellants' invention.

Van Zant fails to remedy the shortcomings of Okuyama et al., specifically the fact that Okuyama et al. forms the oxide layer 14 two layers away from the substrate, not on

the substrate as claimed. Van Zant fails to disclose or suggest in any way that the structure of Okuyama et al. could or should be modified by omitting the two layers, N+-type layer 45 and P+-type layer 46, and forming the oxide layer 14 directly on the substrate 11.

The second missing limitation which the Examiner failed to identify in the cited prior art is the use of ISSG oxidation on both the substrate and the nitride layer. In Okuyama et al. at col. 4, the first oxide layer 14 is not formed by steam oxidation, but is formed by thermal oxidation at 900°C under dry oxygen atmosphere. Okuyama et al. teaches oxidation of a portion of the nitride layer by a heat treatment at 950°C under a steam atmosphere. While Okuyama et al. mentions oxidations in both oxygen and steam atmospheres at col. 2, lines 35-39, this disclosure is in a very general discussion, provides no conditions, times or other details. It is little more than an invitation to experiment, which is not the suggestion required for obviousness. Rather, any person of skill in the art would refer to, be taught by and follow the much more specific and detailed disclosure at column 4, not by the general introductory remarks at column 2. Thus, the disclosure at col. 2 of Okuyama et al. would not lead a person to use steam oxidation to form the first oxide layer 14, even if the layer 14 was formed on the substrate 11, which it clearly is not.

Van Zant teaches a number of different oxidation techniques, one of which is similar to the presently disclosed and claimed ISSG oxidation. In addition to teaching that a "dryox" may be used in which oxygen and hydrogen are fed into an oxidation tube, Van Zant also teaches the use of chlorine-added oxidation. Van Zant does not teach replacing the Okuyama et al. thermal oxidation at 900°C under dry oxygen atmosphere with the "dryox". Furthermore, the Examiner has not identified, and Appellants are not aware of any teaching in Van Zant that the "dryox" should be used to oxidize a nitride layer. Since the layer 14 of Okuyama et al. is not formed by steam oxidation, any teaching of Van Zant to use "dryox" instead of steam is not applicable.

While Okuyama et al. teach oxidation of the nitride layer 15 in a steam atmosphere, there is no suggestion in Van Zant to use the "dryox" for nitride oxidation.

Furthermore, since Okuyama et al. specifically teach oxidation at 900°C in oxygen for the oxide layer 14, but specifically teach oxidation at 950°C in steam for the oxide layer

16, a person of skill in the art would expect there is a reason for the different conditions, and would be taught away from using steam for both oxidations. It would be speculative for the Examiner or the Board to posit any reason for this difference, or why one would not follow the specific teachings of the reference. In other words, the reference teaches two different oxidations on the two different materials, and does not teach that these could be changed. The disclosure at col. 2 does not suggest any interchangeability.

Thus, with respect to the claimed ISSG oxidation of both the substrate and the nitride layer, the Examiner has identified various of the features of Appellants' claimed ISSG oxidation in the cited references, but has failed to identify any teachings which would have lead a person of skill in the art to select from the disclosures of the prior art Appellants' specifically claimed combination, as set forth in Appellants' claims. In order to state a *prima facie* case of obviousness the Examiner must carry this burden. Appellants submit that the Examiner failed to carry this burden.

Thus, the cited references fail to disclose all the features of the claimed invention and all the limitations of Appellants' claims as the invention is set forth therein. There can be no expectation of success where all the limitations of the claimed invention are not shown in the prior art. Or, put another way, there cannot be a reasonable expectation of success in attaining a goal when the elements of the goal are not all defined and arranged. Thus, Appellants submit that the Examiner's conclusion of obviousness is in error, without proper basis, and should be reversed.

In order to state a *prima facie* case of obviousness, the Examiner must show that the cited references disclose all of the limitations of the claims arranged as in Appellants' claims, must show a motivation or suggestion to make the asserted combination and/or modifications necessary to reach the claimed invention, and must show a reasonable expectation of success. The Examiner failed to meet any of these requirements with respect to the presently claimed invention. As noted above, even if the references are taken as asserted by the Examiner, the references fail to teach forming the first oxide layer on the substrate. Instead, Okuyama et al. teaches formation of two intermediate layers, one of N+-type and one of P+-type, on the substrate, and only thereafter forming an oxide

layer on the two intermediate layers, not on the substrate. Similarly, while the references teach various of the elements of the claimed ISSG oxidation, the references fail to show the claimed combination, as claimed. Thus, since the Examiner failed to show all the claim limitations of Appellants' claimed invention, there can be no *prima facie* obviousness.

As noted above, there is no motivation or suggestion, and the Examiner failed to identify a motivation or suggestion to modify the teachings of Okuyama et al. by omitting the two intermediate layers, and there is no motivation or suggestion to modify both the disclosed oxidations of Okuyama et al. with the "dryox" of Van Zant.

For the foregoing reasons, Appellants respectfully submit that all of claims 1 and 5-13 fully distinguish over the asserted combination of Okuyama et al. in view of Van Zant. Accordingly, Appellants respectfully request the Board to reverse the Examiner's rejection of these claims, and to indicate the allowability thereof.

B. THE GENERIC NATURE OF CLAIM 1 REQUIRES THAT CLAIMS 2-4 AND 14-21 BE INCLUDED IN THE EXAMINED CLAIMS, UPON A FINDING THAT CLAIM 1 WOULD NOT HAVE BEEN OBVIOUS OVER THE ASSERTED PRIOR ART IN (A).

Claims 2-4 and 14-21 have been withdrawn from consideration, originally on the basis that they were species of the generic claim 1, and since the Examiner rejected generic claim 1, the Examiner did not examine substantively these claims.

In the final Office Action, the Examiner for the first time asserted that "newly submitted claims 14-21 directed to an invention that is independent or distinct from the invention originally claimed". In Appellants' Reply to Office Action prior to the final Office Action, independent claims 1, 14 and 18 were amended. The amendment of claims 14 and 18 was substantially identical to the amendment of claim 1, was submitted simultaneously, did not change the substance of these claims, and did not change the nature of the invention claimed in these claims.

Despite these inconsistencies in the Examiner's positions, and despite the similarities in the claims, the Examiner failed to identify any reason for this newly asserted

position with respect to allegedly independent inventions. Appellants note that, in the first Office Action, the Examiner did not impose a restriction requirement, but instead imposed an election of species requirement. Thus, at most, there is a single generic invention with two species. Appellants' amendments did not change the classification of the invention claimed. Thus, there is no "invention that is independent or distinct", rather there are only species of the generic claim 1. There is no apparent basis for the Examiner's newly asserted position that claims 14 and 18 are drawn to inventions distinct from the invention to which claim 1 is drawn.

It would appear that the Examiner attempted to bootstrap the different species into different inventions, which is clearly wrong. Claim 1 is drawn to a semiconductor device (generically) including an ONO layer, claim 14 is drawn to a semiconductor device (EEPROM) including an ONO layer and claim 18 is drawn to a semiconductor device (floating gate flash memory) including an ONO layer. Thus, claim 1 is generic to claims 14 and 18.

Since Appellants consider that claim 1 is allowable, the claims 14-21 should be brought back into the case and allowed together with claim 1. Since claims 14-21 are still in the application and were amended the same as claim 1 was amended, the assertion that claim 1 is no longer generic to originally filed or amended claims 14-21 is not understood. Appellants respectfully submit that amended claim 1 remains generic to amended claims 14-21. For the reasons set forth in the following, Appellants respectfully submit that all of the claims are allowable, and thus there is no issue with respect to generic or species claims. Claims 2-4 and 14-21 should be reinstated into this application, and the rejection of all of Appellants' claims should be reversed for the reasons set forth herein.

The Board is respectfully requested to reverse the Examiner's withdrawal of claims 2-4 and 14-21 from the present application.

C. CLAIMS 2-4 AND 14-21 ARE UNOBVIOUS OVER OKUYAMA ET AL, U.S. PATENT NO. 4,918,503, IN VIEW OF VAN ZANT, MICROCHIP FABRICATION, pp. 172-173, 179-182 AND 480-487.

Claims 2-4 and 14-21 contain all or substantially all of the same features as recited in claim 1, and so would not have been obvious over the asserted combination of prior art for at least the same reasons set forth above with respect to claims 1 and 5-13. In addition to those reasons, claims 2-4, 14 and 18 further distinguish over the cited references since these claims specify that the semiconductor device is a two-bit EEPROM device (claims 2, 3 and 14-17) or a floating gate flash memory device (claims 2, 4 and 18-21). The semiconductor device in Okuyama et al. is a DRAM, which is a completely different type of memory device. As is well known, a DRAM is a volatile memory device, which loses its charge and whatever information is stored therein when power is removed. In contrast, the two-bit EEPROM device and the floating gate flash memory devices of the present invention are non-volatile memory devices, from which charge and information are not lost when power is removed. These are additional limitations which the Examiner failed to identify in the cited references. For this additional reason, the Examiner failed to show that the invention of claims 2-4 and 14-21 would have been obvious over the asserted combination of Okuyama et al. and Van Zant.

D. THE EXAMINER APPLIED AN IMPROPER STANDARD, AND FAILED TO PROPERLY STATE A *PRIMA FACIE* CASE OF OBVIOUSNESS.

The Examiner both failed to properly state a *prima facie* case of obviousness, and applied an improper standard of obviousness. To establish a *prima facie* case of obviousness, the burden is on the Examiner to establish facts which substantiate: (1) some suggestion or motivation either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; (2) a reasonable expectation of success that making the asserted modifications and/or combinations would have led to the claimed invention; and (3) that the prior art references must teach or suggest all the claim limitations. See, MPEP 706.02(j)). The

teaching or suggestion to make the asserted modification and/or combination and the reasonable expectation of success must both be found in the prior art, and not be based on Appellant's disclosure. See, In re Vaeck, 20 USPQ2d 1438 (Fed. Cir. 1991).

In the present rejections, the Examiner merely selected particular components from the cited references, ignored other intervening structures and steps, and then concluded that these components can be combined, modified or outright omitted to render Appellants' claims obvious. These are, therefore, improper rejections.

Most importantly, the Examiner failed to show any proper motivation for making the asserted selections, combinations, modifications and omissions in order to arrive at the combination of features recited in Appellants' claims. The Examiner merely asserted that the selected particular components of the references could be selected, combined, modified or omitted, on an *ad hoc* basis, and has not shown any teaching, suggestion or motivation to make the selections, combinations, modifications or omissions.

Specifically, as noted above, the Examiner failed to account for the intervening layers 45 and 46 between the oxide layer and the substrate. These layers preclude the carrying out of the recited steps of Appellants' claims, since it is not possible to carry out a step of "forming a first oxide layer on the silicon surface" in a structure such as that of Okuyama et al. where the silicon surface has been defined as the silicon surface of the semiconductor substrate, as in Appellants' claim 1. The Examiner failed to show the elements of obviousness with respect to the claimed ISSG oxidations.

Furthermore, the Examiner did not show a reasonable expectation of success, which a person of skill in the art must have, in order to make the asserted selections, combinations, modifications and omissions. The Examiner merely selected the steps of forming a first oxide layer, a nitride layer and a top oxide layer, without regard to the specific recitations in Appellants' claims. The Examiner could not show how there could be a reasonable expectation of success, unless the Examiner first showed both a motivation and a way to omit the steps of forming the layers 45 and 46 in Okuyama et al., and showed a motivation and a teaching or suggestion to modify the specific oxidation methods of Okuyama et al. with the "dryox" of Van Zant to obtain the claimed ISSG

oxidations. The Examiner failed to carry this burden. Therefore this is an improper rejection. Accordingly, since the Examiner cannot meet the legal prerequisites to stating a *prima facie* case of obviousness, the rejection should be withdrawn.

"It is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art." *In re Wesley*, 147 U.S.P.Q. 391, 393 (C.C.P.A. 1965). As pointed out in detail above, Okuyama et al. teaches that the oxide layer 14 is formed on two layers, 45 and 46, which are first formed on the substrate 11. Okuyama et al. fails to disclose or suggest, and the Examiner failed to identify, any basis for omitting these layers.

In the case *In re Geiger*, 815 F.2d 686, 2 USPQ2d 1276 (Fed. Cir. 1987), the court found that even though each of the three components of the composition used in the claimed method was conventionally employed in the art, within the meaning of 35 U.S.C. 103, to employ these components in combination for their known functions and to optimize the amount of each additive was not obvious. Rather, rejection of Geiger's claims based on the combination amounted to hindsight reconstruction or at best, an `obvious to try' situation. The facts of *In re Geiger* are similar to the present rejections of all of Appellants' claims. The various steps, found in the references and cited and relied upon by the Examiner in the present application, are variously available in the prior art for arguably similar purposes, but in each case with significant differences, as discussed above. The significant differences require selection and combination, for which there must be a motivation. Even if all the elements could be found in the cited references in the same configuration as claimed, there is no teaching in any of the references to motivate and support the selection and combination of these steps as was done by th Examiner to support the conclusion that Appellants' claimed invention would have been obvious. For this reason, the rejection of Appellants' claims is improper and should be reversed. Appellants respectfully request the Board to reverse the Examiner's rejection of the presently claimed invention.

IX. CONCLUSION

For all these reasons, the rejection of Appellant's claims 1-21 under 35 U.S.C. §103 should be reversed because the asserted combination of references would not have rendered obvious Appellant's claimed process at the time the invention was made. Appellants respectfully request reversal of the Examiner's rejections of Appellants' claimed invention under Section 103.

In the event issues remain in the prosecution of this application, Appellants request that the Examiner telephone the undersigned attorney to expedite consideration and/or allowance of the application. Should a Petition for Extension of Time be necessary for the present Appeal Brief to be timely filed (or if such a petition has been made and an additional extension is necessary) petition therefor is hereby made and, if any additional fees are required for the filing of this paper, the Commissioner is authorized to charge those fees to Deposit Account #18-0988, Docket No. AF01120, AMDSPAF01120.

Respectfully submitted,

RENNER, OTTO, BOISSELLE & SKLAR

22 April 2003
Date

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APPENDIX:
CLAIMS ON APPEAL

1. A process for fabrication of a semiconductor device including an ONO structure, comprising forming the ONO structure by:

providing a semiconductor substrate having a silicon surface;

forming a first oxide layer on the silicon surface;

depositing a silicon nitride layer on the first oxide layer; and

forming a top oxide layer on the silicon nitride layer,

wherein the first oxide layer is formed by an in-situ steam generation oxidation of the silicon surface and the top oxide layer is formed by an in-situ steam generation oxidation of a surface of the silicon nitride layer.

2. The process of claim 1, wherein the semiconductor device comprises a two-bit EEPROM device or a floating gate FLASH device.

3. The process of claim 1, wherein the semiconductor device is a two-bit EEPROM device in which the first oxide layer is a tunnel oxide layer [, and the tunnel oxide layer is formed by an in-situ steam generation oxidation of the silicon surface].

4. The process of claim 1, wherein the semiconductor device is a floating gate EEPROM device in which the first oxide layer is a bottom oxide layer.

5. The process of claim 1, wherein the steps of forming a first oxide layer and forming a top oxide layer are carried out in an RTP apparatus.

6. The process of claim 1, wherein the steps of forming a first oxide layer, depositing a silicon nitride layer and forming a top oxide layer are carried out in a single-wafer cluster tool.

7. The process of claim 1, wherein the silicon nitride is deposited by RTCVD.

8. The process of claim 1, wherein each step of in-situ steam generation oxidation is carried out by providing a hydrogen-containing gas and an oxygen-containing gas to an RTP system or to a single-wafer cluster tool.

9. The process of claim 1, wherein each step of in-situ steam generation oxidation is carried out at a temperature in the range from about 850°C to about 1150°C.

10. The process of claim 1, wherein the step of depositing a silicon nitride layer comprises RTCVD using about 0.5 to 2 slpm ammonia and about 20 to about 50 sccm of a second gas selected from the group consisting of silane and dichlorosilane.

11. The process of claim 10, wherein the RTCVD process comprises a three step sequence including a temperature ramp up step, a deposition step of about 2 minutes, and a cool down step.

12. The process of claim 1, wherein the silicon nitride layer is deposited to a thickness of about 50 to about 300 angstroms.

13. The process of claim 1, wherein the top oxide layer is formed to a thickness of about 50 to about 150 angstroms.

14. A process for fabrication of a semiconductor device, the device including a two-bit EEPROM device including an ONO structure, comprising forming the ONO structure by:

providing a semiconductor substrate having a silicon surface;

forming a tunnel oxide layer overlying the silicon surface by in-situ steam generation oxidation of a portion of the silicon surface;

depositing a silicon nitride layer overlying the tunnel oxide layer; and

forming a top oxide layer overlying the silicon nitride layer by in-situ steam generation oxidation of a portion of the silicon nitride layer.

15. The process of claim 14, wherein the steps of forming a tunnel oxide layer and forming a top oxide layer are carried out in an RTP apparatus which is a component of a single-wafer cluster tool.

16. The process of claim 14, wherein the silicon nitride is deposited by RTCVD.

17. The process of claim 14, wherein each step of in-situ steam generation oxidation is carried out at a temperature in the range from about 850°C to about 1150°C and by providing hydrogen gas and oxygen gas to the RTP apparatus.

18. A process for fabrication of a semiconductor device, the device including a floating gate FLASH structure comprising an ONO structure, comprising forming the ONO structure by:

providing a semiconductor substrate having a floating gate electrode;

forming a bottom oxide layer overlying the floating gate electrode by in-situ steam generation oxidation of a portion of a surface of the floating gate electrode;

depositing a silicon nitride layer overlying the bottom oxide layer; and

forming a top oxide layer overlying the silicon nitride layer by in-situ steam generation oxidation of a portion of the silicon nitride layer.

19. The process of claim 18, wherein the steps of forming a bottom oxide layer, depositing a silicon nitride layer and forming a top oxide layer are carried out in an RTP apparatus which is a component of a single-wafer cluster tool.

20. The process of claim 18, wherein the silicon nitride is deposited by RTCVD.

21. The process of claim 18, wherein each step of in-situ steam generation oxidation is carried out at a temperature in the range from about 850°C to about 1150°C and by providing hydrogen gas and oxygen gas to the RTP apparatus.